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Selected US specifications from IPC sub-class
H04J

(54) Digital data transmission system

(57) The invention concerns a method of transmitting digital data by Time Division Multiplex, in which a justification procedure, either positive or negative, is carried out, and in which data is transmitted in the timeslot allocated for justification in place of the justified bit and is recovered at the receiving end. As discussed, a decision that justification is required is transmitted via multiplexer 105 in justification control digit time slots, AND gate 106 also then being enabled to transmit, in the justification slot, auxiliary data from a FIFO buffer 113.

Fig.1

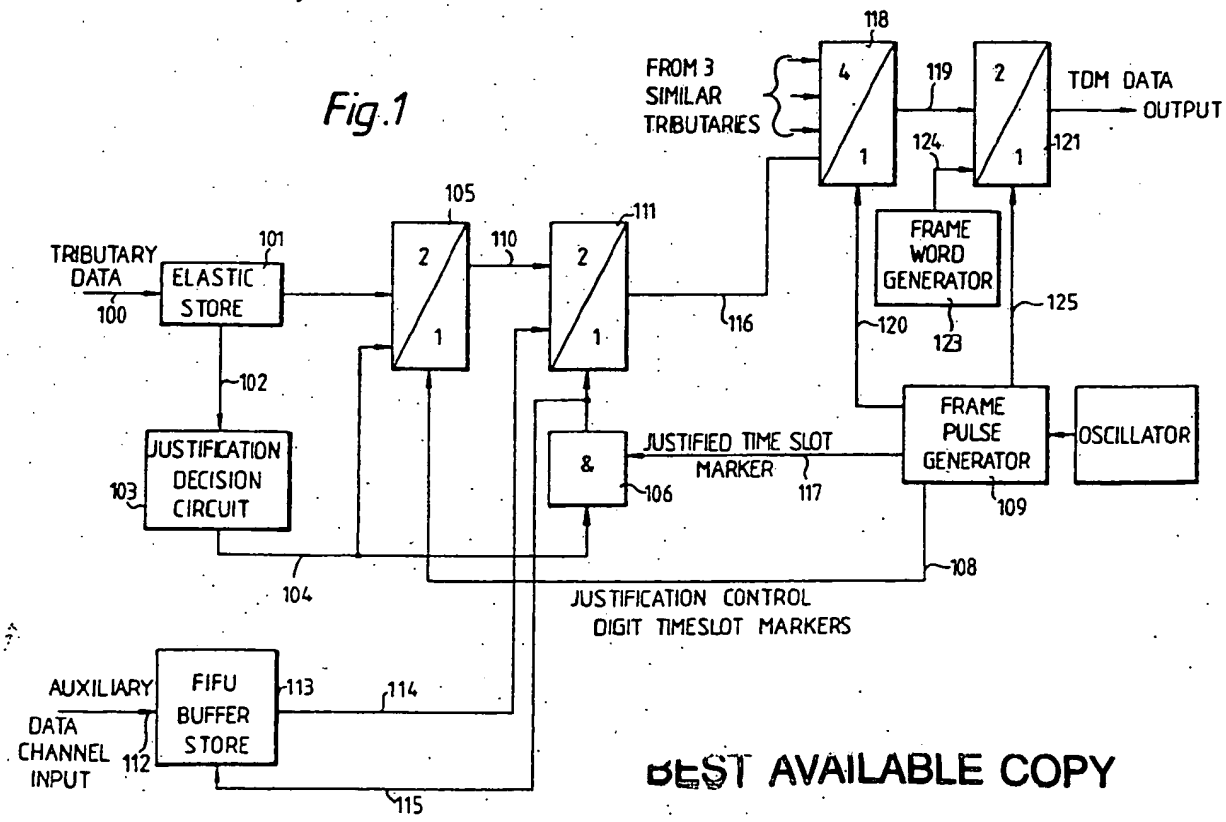
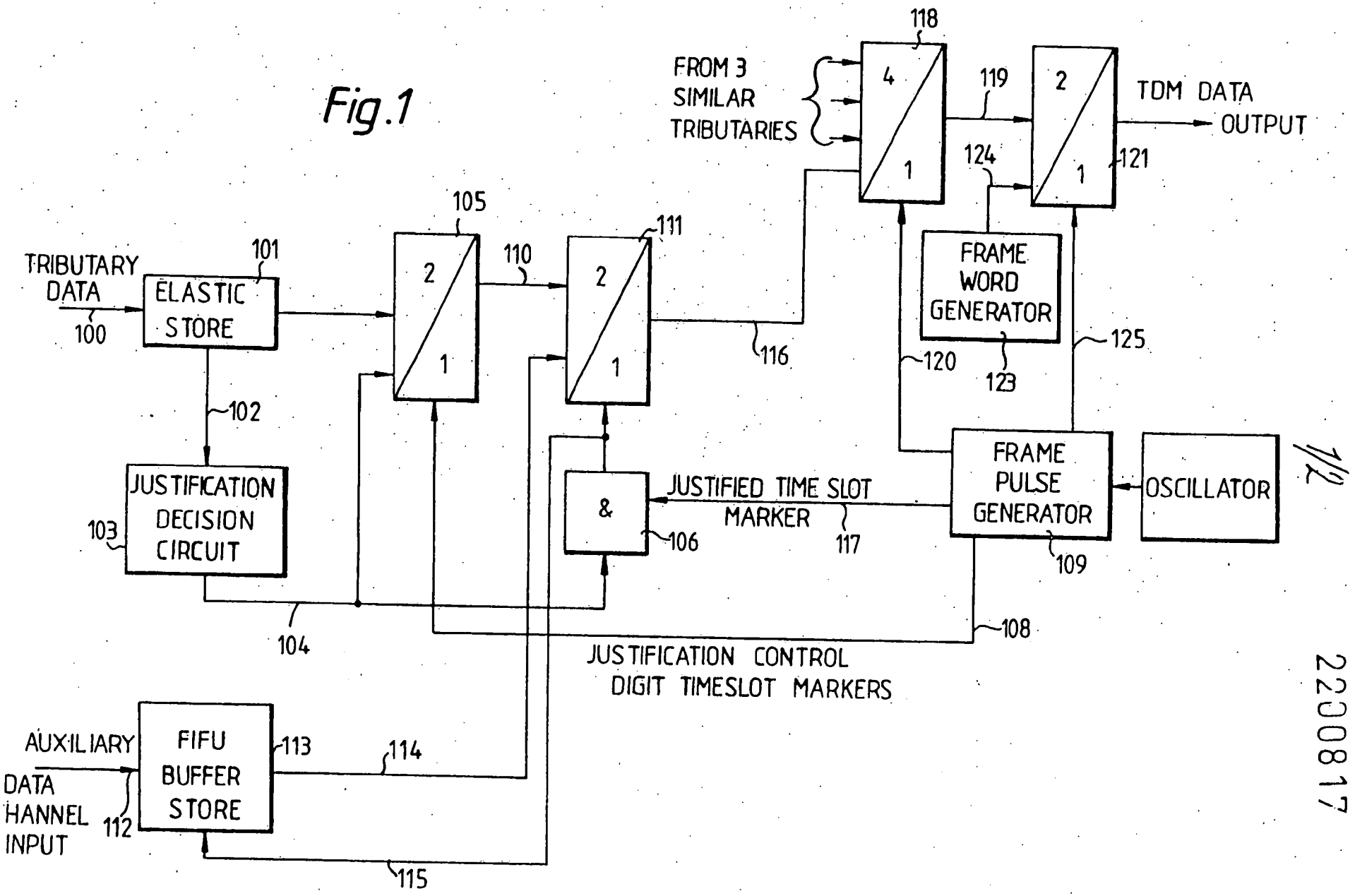


Fig.1



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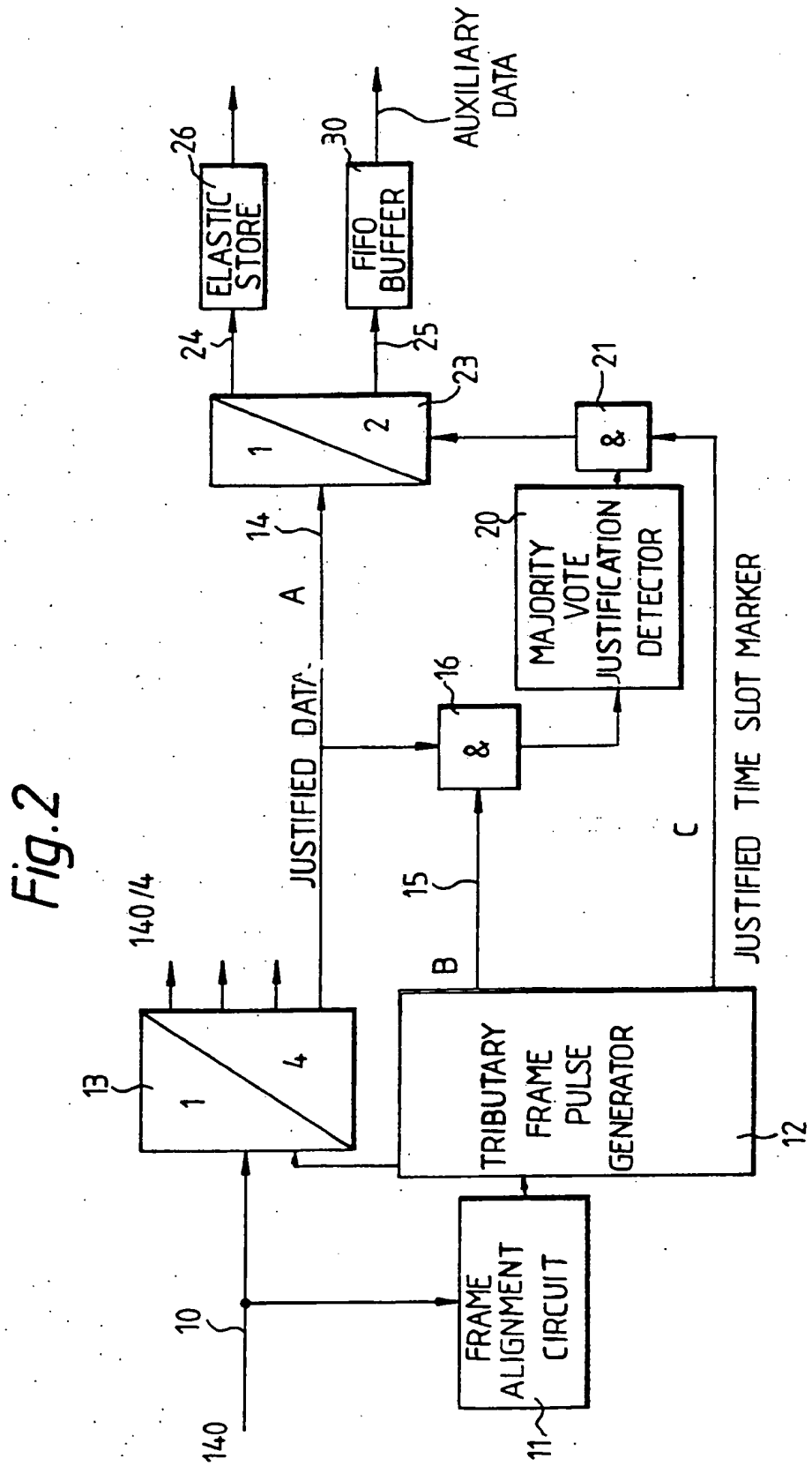
140
10
FRAME ALIGNMENT CIRCUIT
11
TRIBUTARY FRAME PULSE GENERATOR
12
13
1
4
140/4
JUSTIFIED DATA
A
14
15
B
C
JUSTIFIED TIME SLOT MARKER
&
16
MAJORITY VOTE JUSTIFICATION DETECTOR
20
&
21
1
2
23
24
25
ELASTIC STORE
26
FIFO BUFFER
30
AUXILIARY DATA

Fig.2

TED/2969

Digital Data Transmission System

The present invention concerns data transmission systems, and in particular systems in which digital data is transmitted by Time Division Multiplex (TDM).

In TDM multiplexing is used to combine serial bit data streams from a plurality of sources into a single bit stream for more economical transmission. The device for carrying out this process is known as a multiplexer, and the multiplexed high-rate data stream is divided into its constituent lower rate streams by a demultiplexer for the reverse direction of transmission. The combination of a multiplexer and a demultiplexer is known as a muldex, although the transmit multiplexer and the receiver demultiplexer are functionally separate.

The transmit multiplexer accepts a number of inputs, called tributaries, usually consisting of binary data and its associated clock in coded form. The inputs all have the same nominal bit rate, but the actual rates and phases will differ, that is they are plesiochronous. This means that the bit rates of the inputs are close to their nominal rate, but have not other phase or frequency relationship to each other nor to the multi-

plexer output bit rate. Thus not only must the multiplexer perform bit interleaving on the inputs to generate the final high order data stream, but it must also bring the bit rates of the various tributaries to a common rate before bit interleaving. This is achieved by what is known as "justification". There are two types of justification, known respectively as positive and negative justification. Each of these known processes involves the transmission of bits which have no other function than that of ensuring that the tributaries have a common bit rate, and thus involves wasted bandwidth.

The present invention has for an object to utilise this wasted bandwidth.

Accordingly from a first aspect the invention consists in a method of transmitting digital data by Time Division Multiplex, in which a justification procedure, either positive or negative, is carried out prior to transmission, and in which data is transmitted in the timeslot allocated for justification in place of the justified bit and is recovered at the receiving end.

From a second aspect the invention consists in apparatus for transmitting digital data by Time Division Multiplex, including means for justifying the data prior to transmission, and means for inserting data to be recovered at the receiving end in timeslots allocated for justification in place of the justified bit.

The invention also includes receiving equipment for receiving the justified data, and recovering the data transmitted in the justification timeslots.

In order that the present invention may be more readily understood an embodiment thereof will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1 is a block diagram of the transmitting

end of a Time Division Multiplex system according to the present invention, and

Figure 2 is a block diagram of a TDM demultiplexer according to the present invention.

Prior to a description of the drawings, a brief resumé will be given with regard to the procedure of justification in the transmission of digital data by Time Division Multiplex. There are two types of justification, namely positive and negative justification.

During positive justification the input data from each tributary is written into a separate first-in-first-out store known as the transmit elastic store. The data is read in using the clock derived from the tributary input. The data is then read out of all the stores in parallel by a common read-out clock which is derived from a local crystal oscillator. In order to avoid the stores overflowing the read-out clock is arranged to be faster than the fastest expected input clock. However, to avoid the stores being emptied by this faster read-out clock, a pulse is occasionally removed from the read clock for each individual tributary. When this happens, no data bit is read from the relevant store and instead a dummy justified bit is transmitted. In previous systems this dummy bit is removed at the demultiplexer and discarded.

Justified bits are always transmitted in ~~the~~ a justifiable timeslot, one per tributary per frame. This timeslot is known as the Justifi Timeslot.

The sequence of events which is followed is that a decision to justify or not is taken separately for each tributary near the start of a frame, the decision is signalled, and finally the justifiable timeslot is justified or not.

The signal to justify, that is to send a justified bit, is signalled to the distant multiplexer

by a group of bits called the justification service bits so that the justified bit can be removed.

The process in which a data bit is occasionally replaced by a subsequently discarded data bit is called positive justification. Negative justification is used when the read clock in the elastic store has not been arranged to be fast enough always to prevent store overflow. Instead an extra data bit is occasionally removed from the store and transmitted in a spare timeslot.

It will thus be seen that in both positive and negative justification there has to be provision for additional capacity in the main TDM data stream which is merely discarded at the receiving demultiplexer.

Referring to Figure 1 this shows the transmit end of the muldex according to the present invention. In this figure a tributary data stream is transmitted to the elastic store 101 via a line 100. A justification decision circuit 103 determines when justification is required by monitoring the contents of elastic store 101 via line 102. The decision to justify or not is signalled via line 104 to a 2:1 line multiplexer 105 and an AND gate 106. The 2:1 line multiplexer 105 inserts the decision into three timeslots, the justification control digit timeslots, in the tributary data under the control of pulses from the frame pulse generator 109 via line 108. The output of the 2:1 line multiplexer 105 feeds another 2:1 line multiplexer 111 via line 110.

Data from the auxiliary channel input is fed via line 112 to a first-in-first-out (FIFO) buffer store 113. If the justification decision circuit 103 has decided that justification is to occur then a data bit is clocked out of the FIFO buffer store 113 by a signal on line 115. This data bit is inserted via line 114 and 2:1 line multiplexer 111 into the justifiable timeslot in the tributary data appearing on line 110, the resulting

tributary data stream appearing on line 116. The 2:1 line multiplexer 111 is also controlled by the signal on line 115 and is generated by AND gate 106 from the justification decision circuits decision appearing on line 104 and the justified timeslot marker appearing on line 117. The justified timeslot marker is generated by frame pulse generator 109.

Justified data appearing on line 116 is then bit interleaved with similar data from three other tributaries by 4:1 line multiplexer 118, the combined data stream appearing on line 119. The 4:1 line multiplexer is controlled by pulses from the frame pulse generator 109 via line 120. 2:1 line multiplexer 121 inserts a frame word into the data stream appearing on line 119, the resulting TDM data appearing on line 122. The frame word is generated by circuit 123 and is connected by line 124 to the 2:1 line multiplexer 121. The action of 2:1 line multiplexer 121 is controlled by pulses derived from frame pulse generator 109 via line 125.

The TDM data is usually suitably coded before onward transmission to ensure an adequate clock content for correct operation of the receiving equipment.

Referring now to Figure 2 this shows the receive end of the muldex according to the present invention. In this figure TDM data stream is transmitted to the demultiplexer via a line 10. Frame alignment is checked in a frame alignment circuit 11. Checking for frame alignment is a well known procedure and involves detecting the presence of frame alignment words at predetermined intervals. This ensures that the demultiplexer can align itself to the data stream and reconstruct correctly the various tributary streams. The frame alignment circuit 11 will not be described in detail as it is totally conventional. The frame alignment circuit 11 supplies frame pulses to a tributary

frame pulse generator 12. One output of the tributary frame pulse generator 12 is supplied to a 1:4 demultiplexer circuit 13 which provides four output channels of justified data. As the treatment of each of these justified data channels is identical only one, channel 14 will be described.

On channel 4 the tributary frame pulse generator provides three marker pulses which are supplied to one input of an AND-gate 16, the other input of which is the justified data stream on channel 14. The output of AND-gate 16 is fed to a majority vote justification detector circuit 20 so as to identify the presence of a justified data slot. The output of the justification detector circuit is taken to one input of another AND-gate 21, the other input of which is supplied with marker pulses from the tributary frame pulse generator 12. The output of this gate is an indicator as to whether or not there is an auxiliary data bit in the justified timeslot. The output of AND-gate 21 is connected to a 1:2 demultiplexer 23 where the justified data stream on channel 14 is demultiplexed into one channel 24 carrying the tributary traffic and a channel 25 containing the auxiliary data transmitted in the justified timeslot. Channel 24 is connected in a known way to an elastic store 26.

The output from the AND-gate 21 separates the justified timeslot auxiliary data from the justified data and this separated data is supplied to a circuit 30 where it is stored to allow the irregular transmission to be smoothed out.

The above description has been concerned with the transmission and recovery of auxiliary data which has been sent in the justified timeslot where the justification carried out has been positive justification. It will, however, be appreciated that the principle of the data recovery will be the same when the main data stream had been justified by negative justification.

Claims

1. A method of transmitting digital data by Time Division Multiplex, in which a justification procedure, either positive or negative, is carried out, and in which data is transmitted in the timeslot allocated for justification in place of the justified bit and is recovered at the receiving end.

2. Apparatus for transmitting digital data by Time Division Multiplex, including means for justifying the data prior to transmission, and means for inserting data to be recovered at the receiving end in timeslots allocated for justification in place of the justification bit.

3. A data transmission system comprising transmitting apparatus as claimed in Claim 2 in combination with apparatus for receiving the justified data, and means for recovering the data transmitted in the justification timeslots.

4. A digital data transmission system substantially as hereinbefore described with reference to the accompanying drawings.